REMARKS

Claims 1-23 are pending to the present application. By virtue of this response, no claims have been amended and no new claims have been added. Accordingly, claims 1-23 are currently under consideration. Amendment and cancellation of certain claims is not to be construed as dedication to the public of any of the subject matter previously presented.

Interview Summary

The Applicants express their gratitude for the interview with Examiner Lo and Examiner Shah on November 9, 2007. The time and consideration of the Examiners is greatly appreciated.

The substance of the interview is hereby made of record as directed by MPEP § 713.04. The interview of November 9, 2007 took place between Examiner Lo, Examiner Shah, and Thomas Chan, the undersigned agent. No exhibits were shown nor any demonstrations presented. Background of the invention and claim1 of the pending application were discussed. In addition, the Botala reference was discussed in view of the pending Office Action. Applicants presented arguments that the Botala reference does not disclose the elements of the pending claim 1. The details of the arguments are presented in the remarks section below. No agreement was reached.

Claim Rejections – 35 U.S.C. § 103

Claims 1-3, 5-6, 8-16, and 19-23 are rejected under 35 U.S.C. (a) as being unpatentable over Hollander (U.S. Pat. App. Pub. 2002/0073375 A1) in view of Botala et al. (U.S. Patent No. 6,868,513 B1). Applicants respectfully traverse these rejections.

In response, Applicants submit that the Hollander and Botola references, either individually or in combination, do not disclose at least the elements "wherein describing test system configuration comprises specifying a site controller for controlling at least one test module, and wherein each test

module includes vendor-supplied hardware and software components for applying a test to the IC, wherein each vendor-specific software module comprises a module-specific compiler for generating test pattern objects" as recited in the amended claim 1 of the present application. Applicants agree with the Office Action that the Hollander reference "fails to explicitly disclose wherein each test module includes vendor-supplied hardware and software components for applying a test to the IC, wherein each vendor-specific software module comprises a module-specific compiler for generating test pattern objects."

However, the Office Action states the Botala reference allegedly teaches these claim elements (citing column 7, line 4 – column 8, line 3 and Multi_DUT test program 14, Figure 1). Applicants respectfully disagree. Upon a close review of the Botala reference, Applicants note that the Botala reference concerns with mapping multiple DUTs (device-under-test) into pins and channels of the tester system to create test program and pattern data. This is described in Figure 1, Tables 1-7, and their corresponding descriptions from column 2 to column 11 of the Botala specification. Applicants further note that device specific aspect of Botala's solution is based on the device specific Pin Data as shown in item 4 of Figure 1 of the Botala reference. Applicants respectfully submit that person skilled in the art would understand that the Pin Data merely describes hardware specific information about the pins of the DUTs and the pin data does not include vendor-specific software module in the plain meaning of the claim terms. In addition, Applicants respectfully submit that the Botala reference fails to disclose that the vendor-specific software module comprises a module-specific compiler for generating test pattern object. Person skilled in the art would understand that the Pin Data as disclosed in the Botala reference certainly does not include a module-specific compiler, where the module-specific compiler may be used to generate test pattern objects. This is because the Pin Data of the Botala reference cannot perform the function of the module-specific compiler for allowing the integration of modules from different vendors into the tester system.

For the reasons presented above, the cited references fail to disclose the claim elements of pending claim 1 that are used for integrating vendor-supplied hardware and software modules into

an open system architecture using a standard module interface. The standard module interface includes commands that enable users to communicate with a particular hardware module in the system, and commands that enable third-party developers to integrate their own modules into the site controller level framework. The present invention further describes a module-specific compiler for generating test patents objects for applying at least a test to the semiconductor integrated circuit.

The present invention is distinguished from the references cited in the Office Action because the support of vendor-supplied modules with a module-specific compiler for generating test pattern objects allows the semiconductor test system to be an open architecture test system. The objective of such open architecture test system is to solve the long-felt need for a flexible and scalable semiconductor test system. As described in the background section of the pending application, conventional semiconductor test systems are developed in tester manufacturers' proprietary languages. Under such conventional testing environment, each time a new semiconductor integrated circuit needs to be tested, or each time a new test module is needed to test a semiconductor integrated circuit, since both of the new semiconductor integrated circuit and the new test module are typically provided by different vendors, significant amount of time and engineering resources are required to integrated the new test module into the conventional semiconductor test systems. The ability to integrate vendor-specific test modules into the semiconductor test system as described in the pending application addresses this problem in the conventional semiconductor test systems.

In various embodiments of the present application, the specification describes the testing of the Pentium microprocessor designed by Intel Corporation. A person skilled in the art would appreciate that a microprocessor may be used to control many different components in a computer system, such as the memory (DRAM, SRAM, Flash, etc.), I/O (Ethernet, USB, etc.), graphics card, sound card, and hard disk drive (HDD). Each of these components is typically provided by a different vendor. In other words, to test a microprocessor, the semiconductor test system needs to integrated test modules supplied by different vendors. For example, in paragraphs [0095], [0176],

[0194], [0216], and [0219] of the specification, various approaches for developing test programs for testing the Pentium microprocessor are described.

Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollander (U.S. Pat. App. Pub. 2002/0073375 A1) and Botala et al. (U.S. Pat. No. 6,868,513 B1) in further view of National Instruments ("Matrix Switch Expansion Guide").

In response, Applicants assert that claims 4 and 7, which variously depend from the independent claim 1, are allowable for at least the reason that they depend from an allowable independent claim.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hollander (U.S. Pat. App. Pub. 2002/0073375 A1) and Botala et al. (U.S. Pat. No. 6,868,513 B1) in further view of Schauss et al. (U.S. Pat. No. 5,181,201).

In response, Applicants assert that claim 17, which variously depends from the independent claim 1, is allowable for at least the reason that it depends from an allowable independent claim.

REMARKS

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 333772000800. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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